What is claimed is:

1. A flash memory device having an array of floating-gate memory cells, wherein the flash memory device comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter having an input and an output for providing an output signal indicative of a potential level of the input of the sense inverter relative to a threshold point;

a precharge path coupled to the input of the sense inverter for providing a precharge potential to the input of the sense inverter;

a feedback loop interposed between the precharge path and the input node of the sensing device, wherein the feedback loop limits a potential level on the input node of the sensing device to a predetermined maximum potential level; and

a reference current path coupled to the input of the sense inverter for providing a reference current to the input of the sense inverter.

2. The flash memory device of claim 1, wherein the predetermined maximum potential level is less than about 1V.

3. The flash memory device of claim 2, wherein the precharge potential is approximately 3V.

4. The flash memory device of claim 1, wherein the precharge potential is greater than approximately 2.5V and less than approximately 3.7V.

5. The flash memory device of claim 1, wherein the feedback loop presents sufficient resistance to substantially stop charge transfer between the input of the sense inverter and the input node of the sensing device when the potential level of the input node of the sensing device is at the predetermined maximum level and the input of the sense inverter is at the precharge potential.

6. A flash memory device having an array of floating-gate memory cells, wherein the flash memory device comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter;

a first p-channel field-effect transistor coupled between a first potential node and an input of the sense inverter;

a second p-channel field-effect transistor coupled between the first potential node and the input of the sense inverter;

a first n-channel field-effect transistor coupled between the input of the sense inverter and the input node of the sensing device;

a second n-channel field-effect transistor having a gate coupled to the input node of the sensing device, a drain coupled to a gate of the first n-channel field-effect transistor and a source coupled to a second potential node;

a third p-channel field-effect transistor coupled between a third potential node and the gate of the first n-channel field-effect transistor, wherein the third p-channel field-effect transistor has a gate coupled to receive an enable signal; and

a fourth p-channel field-effect transistor coupled between the third potential node and the gate of the first n-channel field-effect transistor, wherein the fourth p-channel field-effect transistor has a gate coupled to receive the enable signal through an inverter.

7. The flash memory device of claim 6, wherein the first potential node and the third potential node are each coupled to receive a supply potential and the second potential node is coupled to receive a ground potential.

8. The flash memory device of claim 6, wherein a current sink developed through the second n-channel field-effect transistor equals the current signal when a predetermined potential is applied to the input node of the sensing device.

9. A flash memory device having an array of floating-gate memory cells, wherein the flash memory device comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter;

a first p-channel field-effect transistor coupled between a first potential node and an input of the sense inverter;

a second p-channel field-effect transistor coupled between the first potential node and the input of the sense inverter;

a first n-channel field-effect transistor coupled between the input of the sense inverter and the input node of the sensing device;

a second n-channel field-effect transistor having a gate coupled to the input node of the sensing device, a drain coupled to a gate of the first n-channel field-effect transistor and a source coupled to a second potential node;

a third p-channel field-effect transistor coupled between a third potential node and the gate of the first n-channel field-effect transistor, wherein the third p-channel field-effect transistor has a gate coupled to receive an enable signal;

a fourth p-channel field-effect transistor coupled between the third potential node and the gate of the first n-channel field-effect transistor, wherein the fourth p-channel field-effect transistor has a gate coupled to receive the enable signal through an inverter;

a fifth p-channel field-effect transistor coupled between the first potential node and the second p-channel field-effect transistor and having a gate coupled to receive the enable signal;

a third n-channel field-effect transistor coupled between the input of the sense inverter and a fourth potential node and having a gate coupled to receive the enable signal; and

a fourth n-channel field-effect transistor coupled between the input node of the sensing device and a fifth potential node and having a gate coupled to receive the enable signal.

10. The flash memory device of claim 9, wherein the fourth potential node and the fifth potential node are each coupled to receive a ground potential.

11. The flash memory device of claim 9, wherein the sense inverter further comprises:

a p-channel stage having a source coupled to a sixth potential node, a drain coupled to an output node of the sensing device and a gate coupled to the input of the sense inverter; and

an n-channel stage having a source coupled to a seventh potential node, a drain coupled to the output node and a gate coupled to the input of the sense inverter.

12. The flash memory device of claim 11, wherein the sixth potential node is coupled to receive a supply potential and the seventh potential node is coupled to receive a ground potential.

13. A flash memory device having an array of floating-gate memory cells, wherein the flash memory device comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter;

a first p-channel field-effect transistor coupled between a first potential node and an input of the sense inverter;

a second p-channel field-effect transistor coupled between the first potential node and the input of the sense inverter;

a first n-channel field-effect transistor coupled between the input of the sense inverter and the input node of the sensing device;

a second n-channel field-effect transistor having a gate coupled to the input node of the sensing device, a drain coupled to a gate of the first n-channel field-effect transistor and a source coupled to a second potential node;

a third p-channel field-effect transistor coupled between a third potential node and the gate of the first n-channel field-effect transistor, wherein the third p-channel field-effect transistor has a gate coupled to receive an enable signal;

a fourth p-channel field-effect transistor coupled between the third potential node and the gate of the first n-channel field-effect transistor, wherein the fourth p-channel field-effect transistor has a gate coupled to receive the enable signal through an inverter;

a p-channel stage having a source coupled to a fourth potential node, a drain coupled to an output node of the sensing device and a gate coupled to the input of the sense inverter; and

an n-channel stage having a source coupled to a fifth potential node, a drain coupled to the output node and a gate coupled to the input of the sense inverter.

14. The flash memory device of claim 13, wherein the fourth potential node is coupled to receive a supply potential and the fifth potential node is coupled to receive a ground potential.

15. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, the memory device having an array of floating-gate memory cells, wherein the memory device further comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter having an input and an output for providing an output signal indicative of a potential level of the input of the sense inverter relative to a threshold point;

a precharge path coupled to the input of the sense inverter for providing a precharge potential to the input of the sense inverter;

a feedback loop interposed between the precharge path and the input node of the sensing device, wherein the feedback loop limits a potential level on the input node of the sensing device to a predetermined maximum potential level; and

a reference current path coupled to the input of the sense inverter for providing a reference current to the input of the sense inverter.

16. The electronic system of claim 15, wherein the predetermined maximum potential level is less than about 1V.

17. The electronic system of claim 16, wherein the precharge potential is approximately 3V.

18. The electronic system of claim 15, wherein the precharge potential is greater than approximately 2.5V and less than approximately 3.7V.

19. The electronic system of claim 15, wherein the feedback loop presents sufficient resistance to substantially stop charge transfer between the input of the sense inverter and the input node of the sensing device when the potential level of the input node of the sensing device is at the predetermined maximum level and the input of the sense inverter is at the precharge potential.

20. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, the memory device having an array of floating-gate memory cells, wherein the memory device further comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter;

a first p-channel field-effect transistor coupled between a first potential node and an input of the sense inverter;

a second p-channel field-effect transistor coupled between the first potential node and the input of the sense inverter;

a first n-channel field-effect transistor coupled between the input of the sense inverter and the input node of the sensing device;

a second n-channel field-effect transistor having a gate coupled to the input node of the sensing device, a drain coupled to a gate of the first n-channel field-effect transistor and a source coupled to a second potential node;

a third p-channel field-effect transistor coupled between a third potential node and the gate of the first n-channel field-effect transistor, wherein the third p-channel field-effect transistor has a gate coupled to receive an enable signal; and

a fourth p-channel field-effect transistor coupled between the third potential node and the gate of the first n-channel field-effect transistor, wherein the fourth p-channel field-effect transistor has a gate coupled to receive the enable signal through an inverter.

21. The electronic system of claim 20, wherein the first potential node and the third potential node are each coupled to receive a supply potential and the second potential node is coupled to receive a ground potential.

22. The electronic system of claim 20, wherein a current sink developed through the second n-channel field-effect transistor equals the current signal when a predetermined potential is applied to the input node of the sensing device.

23. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, the memory device having an array of floating-gate memory cells, wherein the memory device further comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter;

a first p-channel field-effect transistor coupled between a first potential node and an input of the sense inverter;

a second p-channel field-effect transistor coupled between the first potential node and the input of the sense inverter;

a first n-channel field-effect transistor coupled between the input of the sense inverter and the input node of the sensing device;

a second n-channel field-effect transistor having a gate coupled to the input node of the sensing device, a drain coupled to a gate of the first n-channel field-effect transistor and a source coupled to a second potential node;

a third p-channel field-effect transistor coupled between a third potential node and the gate of the first n-channel field-effect transistor, wherein the third p-channel field-effect transistor has a gate coupled to receive an enable signal;

a fourth p-channel field-effect transistor coupled between the third potential node and the gate of the first n-channel

field-effect transistor, wherein the fourth p-channel field-effect transistor has a gate coupled to receive the enable signal through an inverter;

a fifth p-channel field-effect transistor coupled between the first potential node and the second p-channel field-effect transistor and having a gate coupled to receive the enable signal;

a third n-channel field-effect transistor coupled between the input of the sense inverter and a fourth potential node and having a gate coupled to receive the enable signal; and

a fourth n-channel field-effect transistor coupled between the input node of the sensing device and a fifth potential node and having a gate coupled to receive the enable signal.

24. The electronic system of claim 23, wherein the fourth potential node and the fifth potential node are each coupled to receive a ground potential.

25. The electronic system of claim 23, wherein the sense inverter further comprises:

a p-channel stage having a source coupled to a sixth potential node, a drain coupled to an output node of the sensing device and a gate coupled to the input of the sense inverter; and

an n-channel stage having a source coupled to a seventh potential node, a drain coupled to the output node and a gate coupled to the input of the sense inverter.

26. The electronic system of claim 25, wherein the sixth potential node is coupled to receive a supply potential and the seventh potential node is coupled to receive a ground potential.

27. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, the memory device having an array of floating-gate memory cells, wherein the memory device further comprises:

a single-ended sensing device for sensing a programmed state of a floating-gate memory cell, wherein the sensing device has an input node selectively coupled to a floating-gate memory cell, the sensing device further comprising:

a sense inverter;

a first p-channel field-effect transistor coupled between a first potential node and an input of the sense inverter;

a second p-channel field-effect transistor coupled between the first potential node and the input of the sense inverter;

a first n-channel field-effect transistor coupled between the input of the sense inverter and the input node of the sensing device;

a second n-channel field-effect transistor having a gate coupled to the input node of the sensing device, a drain coupled to a gate of the first n-channel field-effect transistor and a source coupled to a second potential node;

a third p-channel field-effect transistor coupled between a third potential node and the gate of the first n-channel field-effect transistor, wherein the third p-channel field-effect transistor has a gate coupled to receive an enable signal;

a fourth p-channel field-effect transistor coupled between the third potential node and the gate of the first n-channel field-effect transistor, wherein the fourth p-channel field-effect transistor has a gate coupled to receive the enable signal through an inverter;

a p-channel stage having a source coupled to a fourth potential node, a drain coupled to an output node of the sensing device and a gate coupled to the input of the sense inverter; and

an n-channel stage having a source coupled to a fifth potential node, a drain coupled to the output node and a gate coupled to the input of the sense inverter.

28. The electronic system of claim 27, wherein the fourth potential node is coupled to receive a supply potential and the fifth potential node is coupled to receive a ground potential.